HyperTransport™ Technology Power Management Overview

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AMD

Platform Conference
Direction • Design • Perspective • Analysis

Why should we care about power management?

- Increase battery powered run time and reduced “skin” temperature in a notebook PC
- Quieter operation in a desktop PC
- Allow for higher density server farms
- Improve system reliability
- Save ourselves and our companies money by reducing electric bills
- Help prevent “rolling blackouts”

HyperTransport™ Technology Power Management Goals

- Reduce component / system cost
- Work with existing operating systems
- Meet the needs of all classes of systems from mobile systems to multi-processor servers
- ACPI compliant
- Enable advances in power management

HyperTransport™ Technology Delivers

- **Message Based Power Management**
  - Legacy pins like STPCLK#, and others required to differentiate between power states have been converted to messages.
  - Reduced pin count = Reduced cost
- **ACPI compliant power management designed to be suitable for all classes of systems from notebooks to Servers.**
- **HyperTransport provides link (Bus) power management.**
- **HyperTransport link width and frequency are scalable.**

Message Based Power Management

- **STPCLK System Message carries a 3 bit "System Management Action Field" (SMAF)**
  - Differentiates between all of the various reasons that STPCLK is asserted.
- **Stop Grant broadcast also contains the SMAF**
  - Informs each HyperTransport™ device why Stop Grant was entered
  - Devices have programmable responses that are associated with a given SMAF code.

ACPI State Support By Class

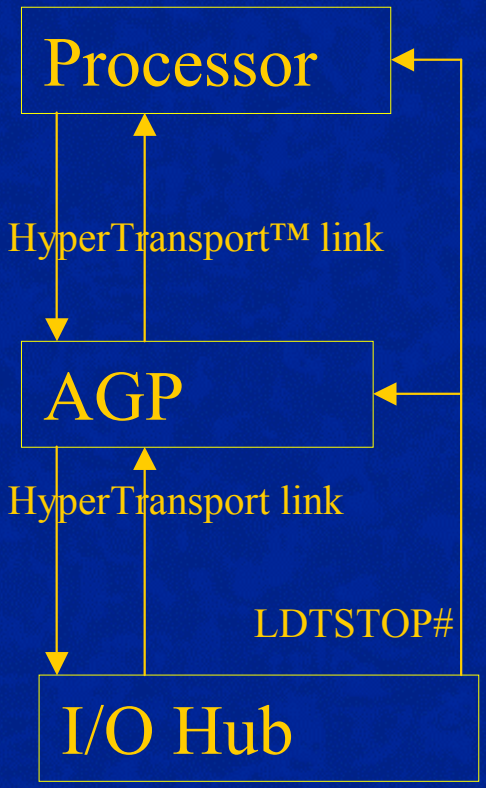
ACPI State	Mobile Systems	Uni-Processor Desktop PCs	Multi-Processor Systems
S0/C0: Processor performance state transitions (AMD PowerNow!™ Technology)	Yes	Yes	Yes
S0/C0: Thermal clock throttling (hardware enforced)	Yes	Yes	Yes
S0/C0: Thermal clock throttling (operating system enforced)	Yes	Yes	CPU specific
S0/C1: Halt	Yes	Yes	Yes
S0/C2: Stop Grant Caches snoopable	Yes	Yes	CPU specific
S0/C3: Stop Grant Caches not snoopable	Yes	No	No
S1: Stand By (Powered On Suspend)	Yes	Yes	Yes
S3: Stand By (Suspend to RAM)	Yes	Yes	Yes
S4: Hibernate (Suspend to Disk)	Yes	Yes	Yes
S5: Shut Down, Turn Off (Soft Off)	Yes	Yes	Yes

Link/Bus Power Management

- **HyperTransport™ link (Bus) power management is enabled by the LDTSTOP# signal.**
- **LDTSTOP# assertion causes:**
  - HyperTransport devices to disconnect their HyperTransport links
  - HyperTransport devices can easily gate large sections of their clock grids because all that needs to be monitored is LDTSTOP#
  - Allows for HyperTransport link receivers to be tri-stated (key mobile power savings feature - without this differential signal terminations constantly consume power.)
- **LDTREQ# provides C3 exit functionality**
  - Assertion is analogous to PCI Bus master REQ# signal in that it forces ACPI BM_STS bit to be set forcing exit from C3.

C3 State Example

- Operating System sets ARB_DIS bit, reads PM_TMR, reads PLVL_3 register in I/O Hub
- I/O Hub sends STPCLK message with SMAF code indicating C3
- Processor Enters Stop Grant and issues Stop Grant special cycle with C3 SMAF code
- Graphics solution sees Stop Grant with C3 SMAF and is conditioned to take appropriate PM response when LDTSTOP# is asserted.
- I/O Hub receives Stop Grant and asserts LDTSTOP#
- HyperTransport™ devices disconnect and tri-state their HyperTransport links.
- With the HyperTransport links disconnected after LDTSTOP# assertion, the processor and Graphics solution are isolated from other devices in the system, and take the programmed power management action associated with C3 (gate clocks for example).



Call To Action

- Join the HyperTransport™ Consortium
- Join a HyperTransport Consortium Working Group
- Visit the HyperTransport web site, there will be a Power Management White Paper soon
- Look forward to using power efficient HyperTransport Technology based components